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- **High-Speed Drive Controller for PNP Power Transistor**
- Internal-Regulator Provides a Stable 1.5 V **Reference Supply**
- Low Start-Up Voltage 3.1 V

- **Internal Short-Circuit Protection**
- **Internal Undervoltage Lockout Protection**
- **Internal Shut-Down Circuit by Channel**
- **Controllable Base Current of External Transistor**

description

The TL1464I incorporates on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, the TL1464l contains an on-chip 1.5 V regulator, four error amplifiers, an oscillator, two dead-time comparators, undervoltage lockout circuitry, short circuit protection, standby control circuitry, and output circuits.

The external speed-up capacitors provide exceptional rise and fall time performance for the PNP power transistor.

The TL1464I operates from 3.1 V supply voltage and 2 pair of four-outputs (CH-1/CH-3, CH-2/CH-4 the same period) at the inverse phase of each other. As a result, the TL1464I provides high-efficiency power supply.

FUNCTION TABLE

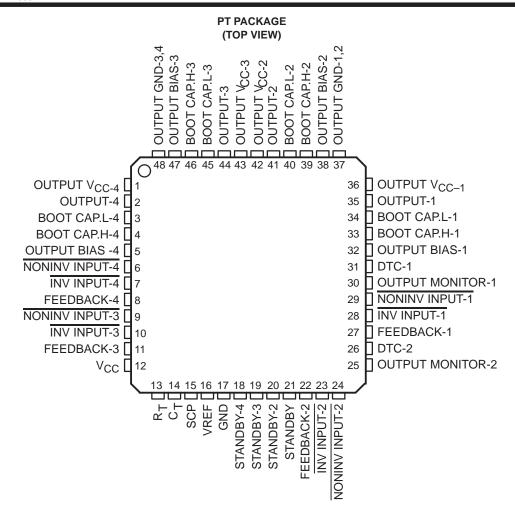
ı	NPUTS		(OUTPUT FUNCT	IONS	
STANDBY	STANDBY-2 TO4	VREF	OUTPUT-1	OUTPUT-2	OUTPUT-3	OUTPUT-4
V _I ≤ 0.4 V	$V_{I} \leq 0.4 \text{ V}, V_{I} \geq 2.4 \text{ V}$	L	OFF	OFF	OFF	OFF
V ₁ > 2.4 V	V _I ≥ 2.4 V	Н	ON	ON	ON	ON
V _I ≥ 2.4 V	V _I ≥ 0.4 V	Н	ON	See Note	See Note	See Note

NOTE: When the STANDBY input is high (≥ 2.4 V), OUTPUT-2 to 4 are controlled individually. If STANDBY-2 input is low (≤ 0.4 V), OUTPUT-2 is turned off. When CH-2 standby mode is released, CH-2 can do the soft-start function.

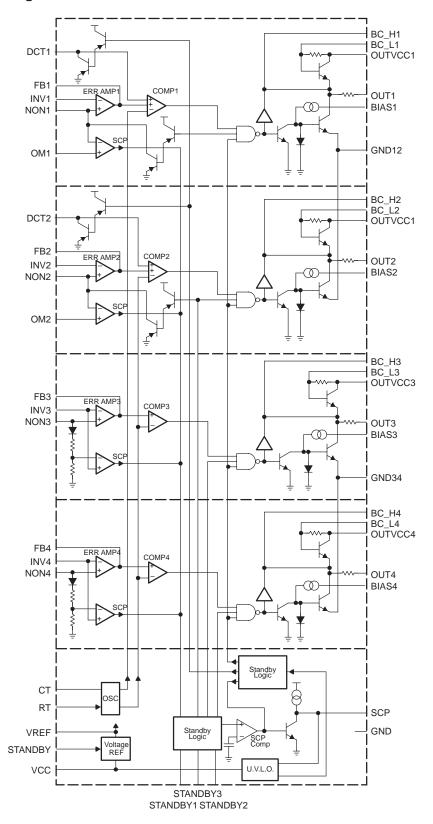


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





functional block diagram





Terminal Functions

TERMINAL				
NAME	NO.	1/0	DESCRIPTION	
BOOT CAP.H-1	33		Post of the constitution of the constitution (OUA)	
BOOT CAP.L-1	34		Boot-strap capacitor connect pin (CH-1)	
BOOT CAP.H-2	39		ot-strap capacitor connect pin (CH-2)	
BOOT CAP.L-2	40		Boot-strap capacitor connect pin (CH-2)	
BOOT CAP.H-3	46		oot-strap capacitor connect pin (CH-3)	
BOOT CAP.L-3	45		Boot-strap capacitor connect pin (CH-3)	
BOOT CAP.H-4	4		Post strong consider connect sin (CU 4)	
BOOT CAP.L-4	3		Boot-strap capacitor connect pin (CH-4)	
CT	14		Timing capacitor connect pin	
DTC-1	31		Dead-time control input pin (CH-1)	
DTC-2	26		Dead-time control input pin (CH-2)	
FEEDBACK-1	27		Error amplifier output pin (CH-1)	
FEEDBACK-2	22		Error amplifier output pin (CH-2)	
FEEDBACK-3	11		Error amplifier output pin (CH-3)	
FEEDBACK-4	8		Error amplifier output pin (CH-4)	
GND	17		Ground pin	
INV INPUT-1	28		Error amplifier inverting input pin (CH-1)	
INV INPUT-2	23		Error amplifier inverting input pin (CH-2)	
INV INPUT-3	10		Error amplifier inverting input pin (CH-3)	
INV INPUT-4	7		Error amplifier inverting input pin (CH-4)	
NONINV INPUT-1	29		Error amplifier noninverting input pin (CH-1)	
NONINV INPUT-2	24		Error amplifier noninverting input pin (CH-2)	
NONINV INPUT-3	9		Error amplifier noninverting input pin (CH-3)	
NONINV INPUT-4	6		Error amplifier noninverting input pin (CH-4)	
OUTPUT-1	35		Output pin (CH-1)	
OUTPUT-2	41		Output pin (CH-2)	
OUTPUT-3	44		Output pin (CH-3)	
OUTPUT-4	2		Output pin (CH-4)	
OUTPUT BIAS-1	32		Output ON current setup pin (CH-1)	
OUTPUT BIAS-2	38		Output ON current setup pin (CH-2)	
OUTPUT BIAS-3	47		Output ON current setup pin (CH-3)	
OUTPUT BIAS-4	5		Output ON current setup pin (CH-4)	
OUTPUT GND-1,2	37		Output ground pin (CH-1,2)	
OUTPUT GND-3,4	48		Output ground pin (CH-3,4)	
OUTPUT MONITOR-1	30		Output monitor comparator input pin (CH-1)	
OUTPUT MONITOR-2	25		Output monitor comparator input pin (CH-2)	
OUTPUT V _{CC-1}	36		Output supply pin (CH-1)	
OUTPUT V _{CC-2}	42		Output supply pin (CH-2)	
OUTPUT V _{CC-3}	43		Output supply pin (CH-3)	
OUTPUT V _{CC-4}	1		Output supply pin (CH-4)	
R _T	13		Timing resistor connect pin	
SCP	15		Short-circuit protection capacitor connect pin	



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Terminal Functions (Continued)

TERMINAL		.,,	DECORPORTION
NAME	NO.	1/0	DESCRIPTION
STANDBY	21		Output-1 to 4 control pin. Input L level voltage (0.4 V max). All outputs function and VREF are shutdown.
STANDBY-2	20		Output-2 control pin. Input L level voltage (0.4 V max), output-2 function is shutdown.
STANDBY-3	19		Output-3 control pin. Input L level voltage (0.4 V max), output-3 function is shutdown.
STANDBY-4	18		Output-4 control pin. Input L level voltage (0.4 V max), output-4 function is shutdown.
Vcc	12		Power supply pin

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V _{CC} (see Note 1)	13 V
Amplifier input voltage, V _{IC}	
Output voltage, V _O	13 V
Peak output current (sink), I _(SINK)	100 mA
Peak output current (source), I _{SOURCE}	1 A
Continuous total dissipation at (or below) 25°C free-air temperature (unit), P _D	
Continuous total dissipation at (or below) 25°C free-air temperature (using board), PD	
(see Note 2)	1315 mW
Operating free-air temperature range, T _A	−20°C to 75°C
Storage temperature range, T _{stq}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage4 value are with respect to network ground terminal.

2. Using $t1.6 \times 50 \times 50$ mm glass epoxy resin.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		3.1		12	V
Amplifier input voltage V/ce	CH-1,2	-0.1		V _{CC} -1.8	V
Amplifier input voltage, V _{IC}	CH-3,4	0		V _{CC} -1.8	V
Standby input voltage V. (pinc 18, 10, 20, 21)	H level	2.4		Vcc	V
Standby input voltage, V _I (pins 18, 19. 20. 21) L level Output voltage, V _O Current into feedback terminal, I _(CAMP) Feedback resistor, R _(NF)	L level			0.4	V
Output voltage, V _O				12	V
Current into feedback terminal, I(CAMP)				-45	μΑ
Feedback resistor, R _(NF)		100			kΩ
Boot-strap capacitor, C(BOOT)		100	500		pF
Bias resistor, R(BIAS)		1.2		20	
Bias capacitor, C(BIAS)			30	200	pF
Timing resistor, R _(T)		7		50	kΩ
Timing capacitor, C _(T)		68		1000	рF
Oscillation frequency, f(OSC)		0.05		2	MHz
Operating free-air temperature, TA		-20		75	°C

TL1464I QUAD PULSE-WIDTH-MODULATION CONTROL CIRCUIT

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electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 6 \text{ V}$, f = 1 MHz (unless otherwise noted)

reference section

	PARAMETER	TEST CO	NDITIONS	MIN	TYP	MAX	UNIT
V _{ref}	Output voltage (pin 16)	T _A = 25°C,	$I_{(OR)} = -1 \text{ mA}$	1.485	1.50	1.515	V
R(EGIN)	Input regulation	$V_{OS} = 3.1 \text{ V to } 12 \text{ V},$	$I_{(OR)} = -1 \text{ mA}$		2	12.5	mV
R _(EFL)	Output regulation	$I_{(OR)} = -0.1 \text{ mA to } -1$	mA		1	7.5	mV
V(RTC1)	Output voltage change with temperature	T _A = 20°C to 25°C			-0.2%	±2%	
R _(RTC2)	Output voltage change with temperature	$T_A = 25^{\circ}C$ to $75^{\circ}C$			-0.2%	±2%	
los	Short-circuit output current	V _{ref} = 0 V		4	8		mA

undervoltage lockout section

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIH	Upper threshold voltage			2.7		V
VIL	Lower threshold voltage	T. 259C		2.5		V
V _{hys}	Hysteresis	T _A = 25°C	0.1	0.2		V
٧R	Reset threshold voltage (V _{CC})		2.2	2.3		V

output voltage monitor section

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IO(M)} Input offset voltage		T _A = 25°C (CH-1,2)		0		
	V _I = 1.5 V (pins 6 and 9), T _A = 25°C (CH-3,4)		10.5		V	
I _(BOM)	Input bias current	V _I = 0 V		-200	-500	nA
V _(IOM)	Input voltage range	V _{CC} = 3.1 V ~ 12 V	0 to V _{CC} -1.8			V

protection control section

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _(tPC)	Input threshold voltage (pin 15)	T _A = 25°C	1.45	1.50	1.55	V
V _(stby)	Standby voltage (pin 15)		40	70	100	mV
VI	Latched input voltage (pin 15)			10	30	mV
I _(bPC)	Input source current (pin 15)	T _A = 25°C	-1	-3	-6	μΑ

oscillator section

	PARAMETER	TEST CONDITIONS	MIN TYP MAX	UNIT
f(OSC)	Frequency	$C_t = 100 \text{ pF}, \qquad R_t = 10 \text{ k}\Omega$	1	MHz
f(dev)	Standard deviation of frequency	All values are constant	7%	
f(dV)	Frequency change with voltage	V _{CC} = 3 V ~ 12 V	1%	
f(dT1)	Frequency change with temperature	$T_A = 20^{\circ}C$ to $25^{\circ}C$	-0.5% ±4%	
f(dT2)	Triequency change with temperature	$T_A = 25^{\circ}C$ to $75^{\circ}C$	0.5% ±4%	



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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 1 MHz (unless otherwise noted) (continued)

dead-time control section

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _(Idt)	Input current			-1	-4	μΑ
I _(dt)	Latched mode sink current	T _A = 25°C	0.3	1	2	mA
V _(dt)	Latched input voltage	I _(dt) = 100 μA			0.5	V
VIO	Input threshold voltage	Zero duty cycle	0.6	0.7	0.8	V
V _(tt00)	Tilput tilleshold voltage	100% duty cycle	1.3	1.4	1.5	v

error-amplifier section

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIO	Input offset voltage		V _O = 1 V			±10	mV
I _{IO}	Input offset current		V _O = 1 V			±100	nA
I _{IB}	Input bias current		V _O = 1 V		-200	-500	nA
\/	Common-mode input voltage	CH-1,2	Vaa 24V 42V	-0.1 to V _{CC} -1.8			V
VICR		CH-3,4	V _{CC} = 3.1 V ~ 12 V	0 to V _{CC} -1.8			V
A _(v)	Open-loop voltage amplification		R _I = 200 kΩ	60	75		dB
B1	Unity-gain bandwidth				6		MHz
CMRR	Common-mode rejection ratio		$V_{IC} = -0.1 \text{ V} \sim V_{CC} - 1.8 \text{ V}$	60	80		dB
V _{OM+}	Maximum autout valtage aving			V _{ref} -0.1			V
V _{OM} –	Maximum output voltage swing					0.2	V
I _{O(vr+)}	Output current (sink)		$V_{ID} = -0.1 \text{ V}, V_{O} = 1.25 \text{ V}$	0.5	1		mA
1 +	Sink current (pin 24) (standby mo	ode)	V _I = 0.3 V (pin 24) V _I = 0 V (pin 20)	0.1	0.5		mA
I _{OM} _	Output current (source)		$V_{ID} = 0.1 \text{ V}, \qquad V_{O} = 0.75 \text{ V}$	-45	-85		μΑ

output section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I/SINK) Output current (sink)	$R(BIAS) = 2.4 k\Omega$	15	20	25	
(SINK) Output current (sink)	$R_{(BIAS)} = 5.8 \text{ k}\Omega$	7.5	10	12.5	mA

total device

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{O(CS)}	Standby supply current	Standby pin input voltage = 0 V		1	200	μΑ
I _{O(CA)}	Average supply current	$R_t = 10 \text{ k}\Omega$		4	7	mA

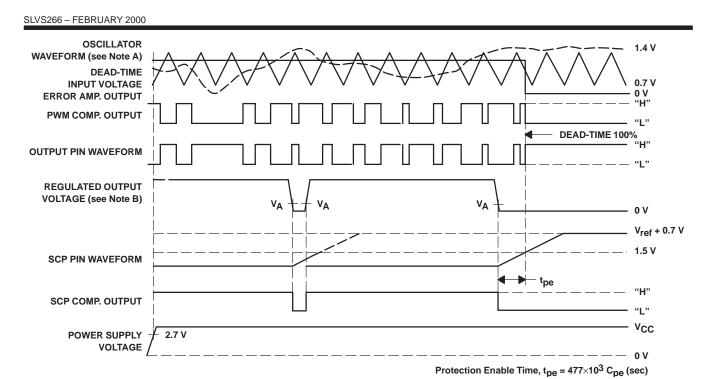


Figure 1. Timing Diagram (CH-1/CH-2)

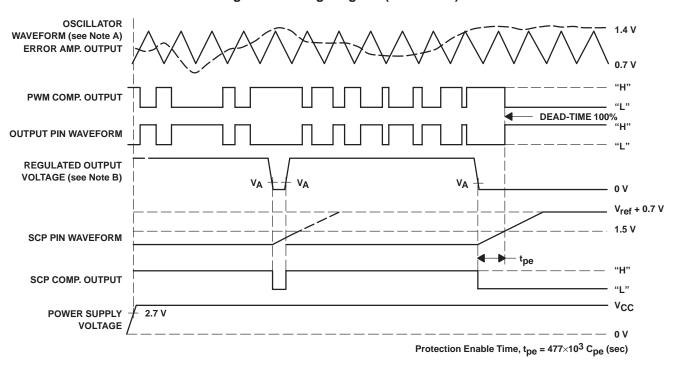


Figure 2. Timing Diagram (CH-3/CH-4)

NOTES: A. Oscillator waveform of CH-1 and CH-2 is inverting output each other.

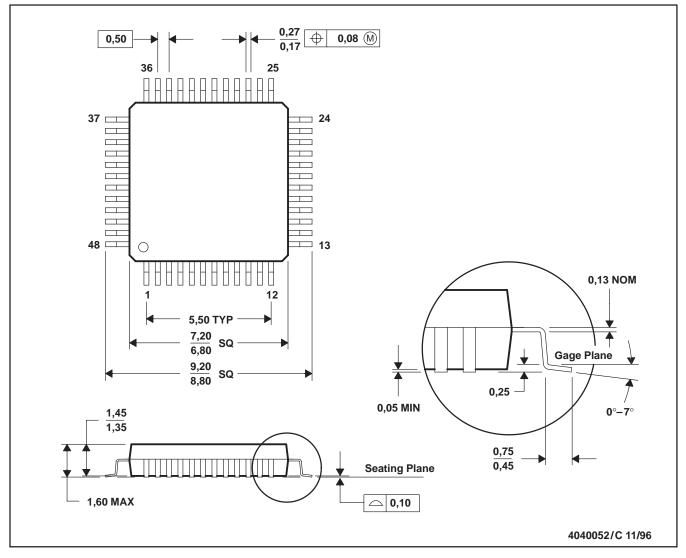
B. Va = input voltage of pin 29 (pin 24)



MECHANICAL DATA

PT (S-PQFP-G48)

PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-026
- D. This may also be a thermally enhanced plastic package with leads conected to the die pads.





com 6-Dec-2006

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TL1464IPT	ACTIVE	LQFP	PT	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1464IPTG4	ACTIVE	LQFP	PT	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1464IPTR	ACTIVE	LQFP	PT	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1464IPTRG4	ACTIVE	LQFP	PT	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

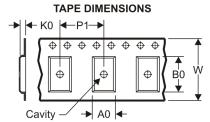
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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL1464IPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL1464IPTR	LQFP	PT	48	1000	346.0	346.0	33.0

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